Wire Capacitance and Reversible Logic

Draft

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Overview



CMOS and reversible circuits respond to wire capacitance differently

- In CMOS, big transistors are required to drive long wires, raising power consumption
- In reversible circuits, big transistors lower the dissipation of long wires

Subsequent slides

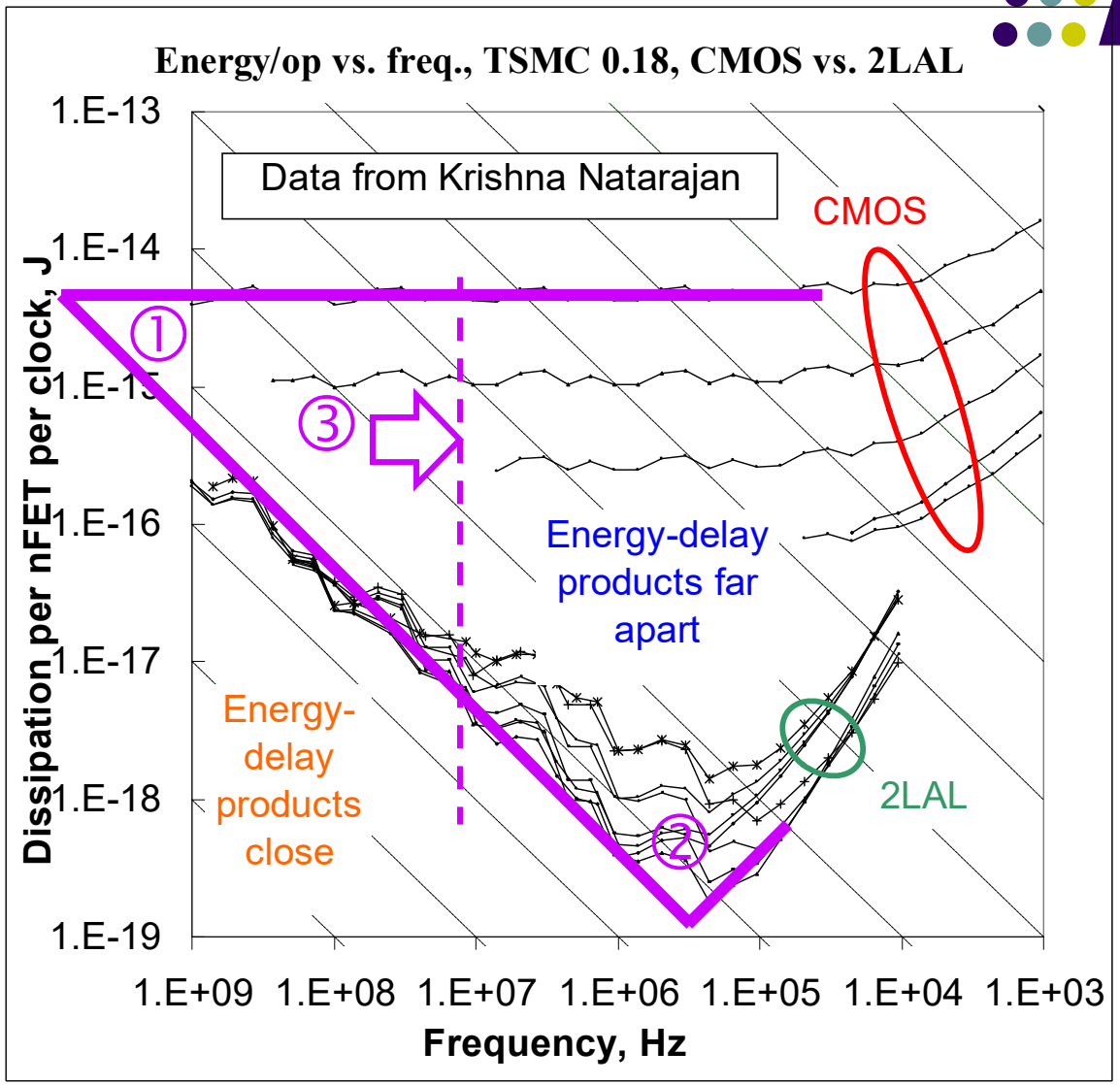
- show the traditional energy comparison between CMOS and reversible logic
- include five-slide animation showing a hidden variable is responsible for a 10× difference in the conclusion
- present math describing the issue

CMOS vs. Reversible Logic (not right)

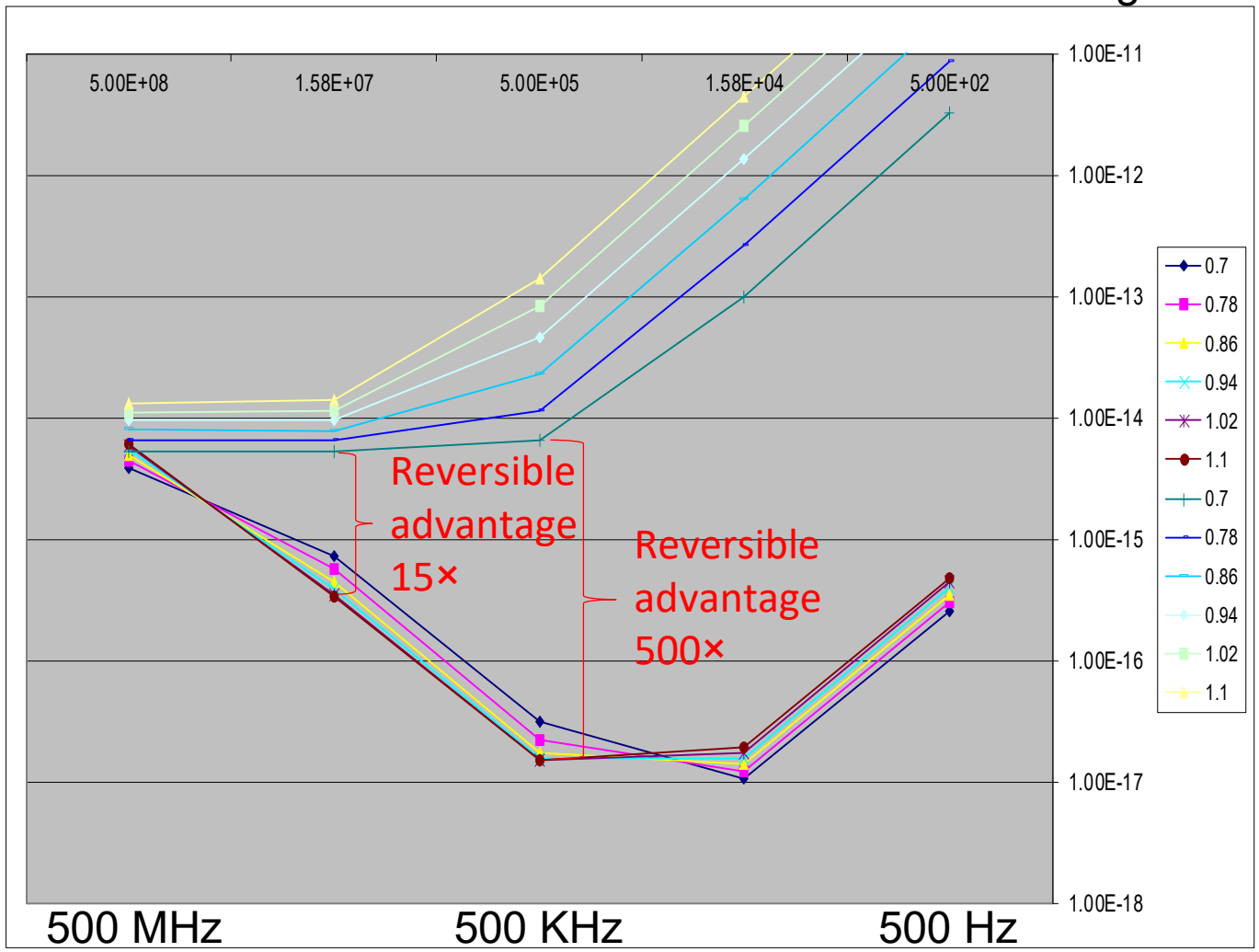
① Flat CMOS line intersects slope -1 reversible line at about CMOS's top speed

② Reversible circuits continue at energy $\propto 1/\tau$ until static leakage dominates

③ Read energy efficiency advantage at application's clock rate

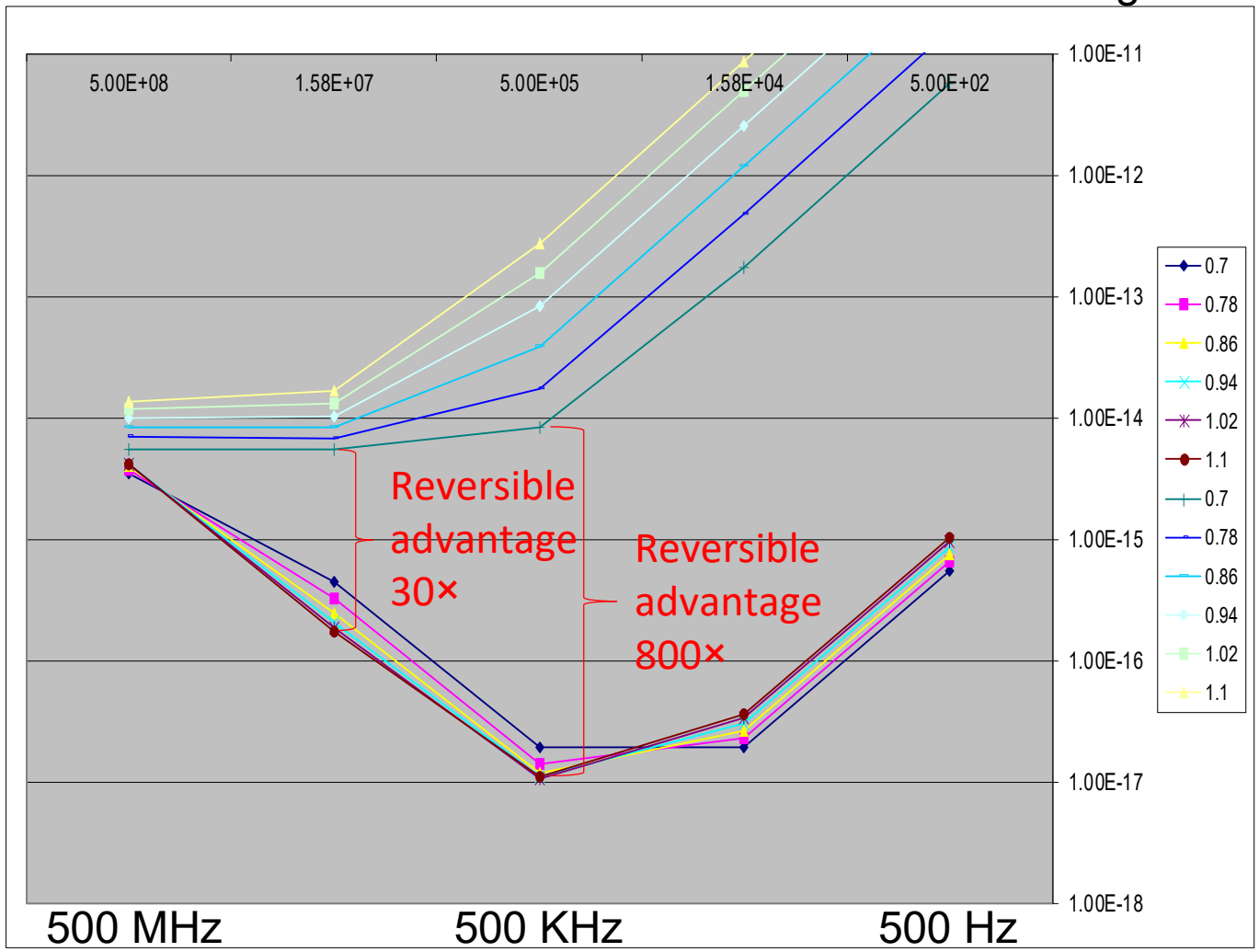


Overlay animation



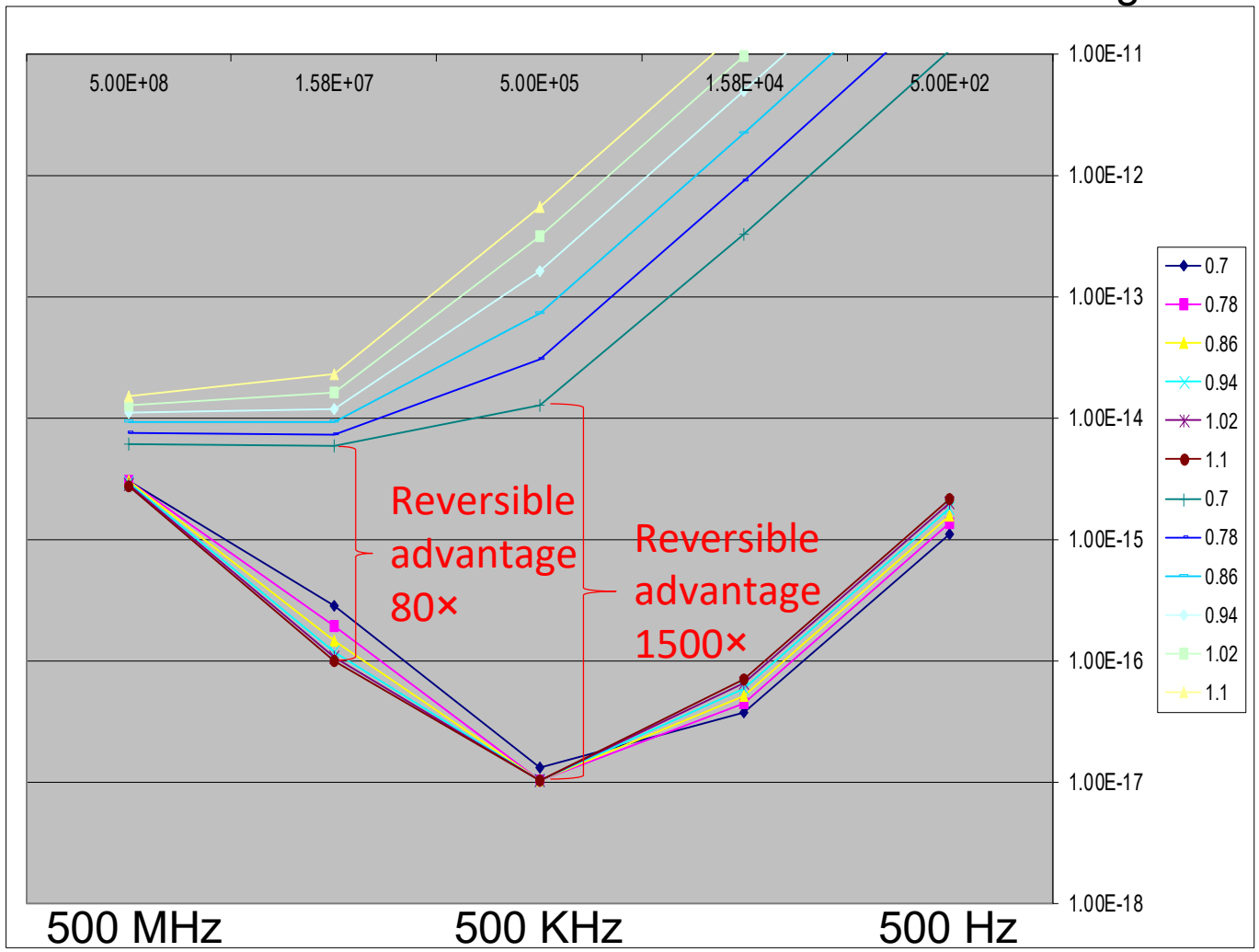
360 nm width; transistors are FDSI 90 nm from Lincoln Labs (public information); C_w = 10 fF

Overlay animation



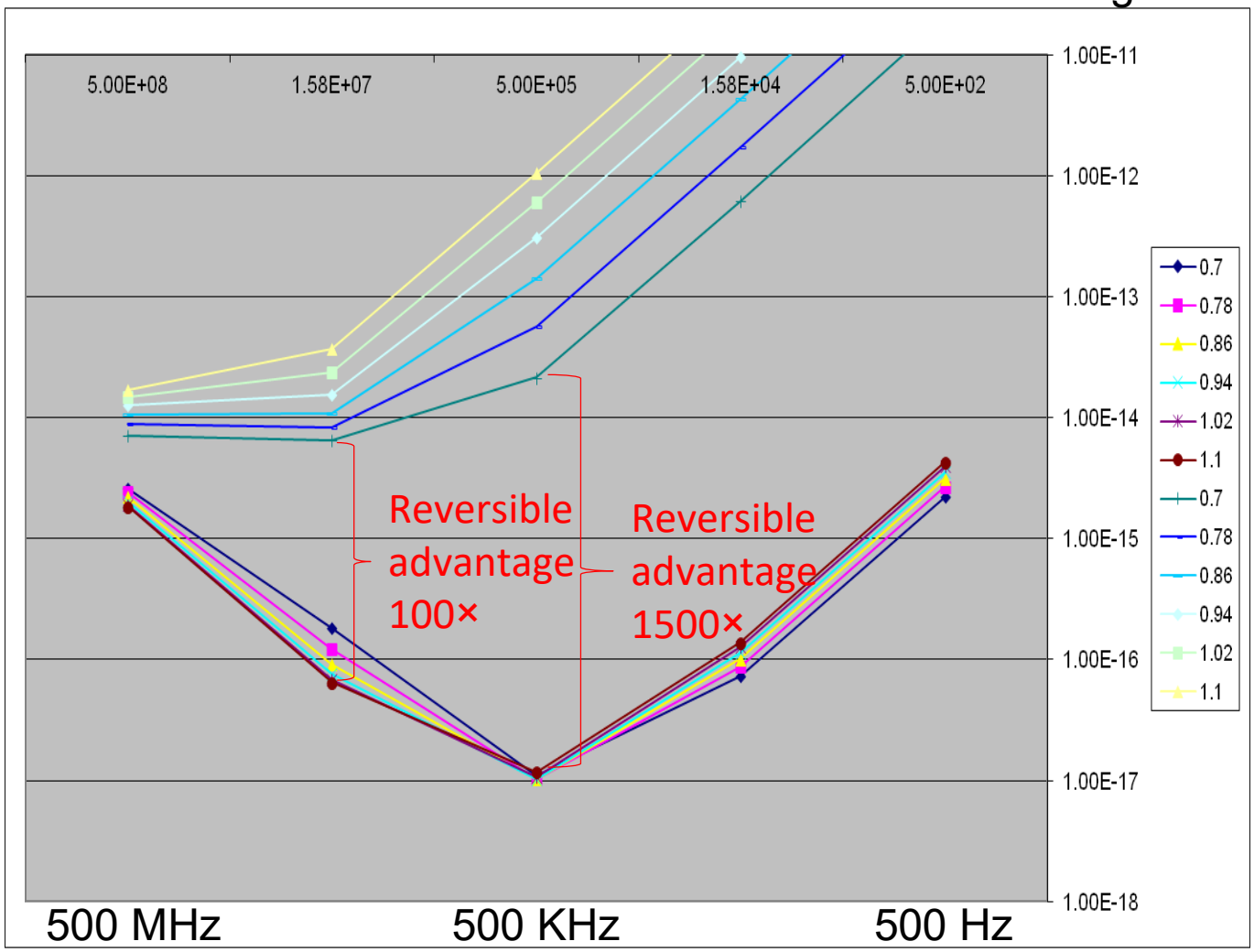
720 nm width

Overlay animation



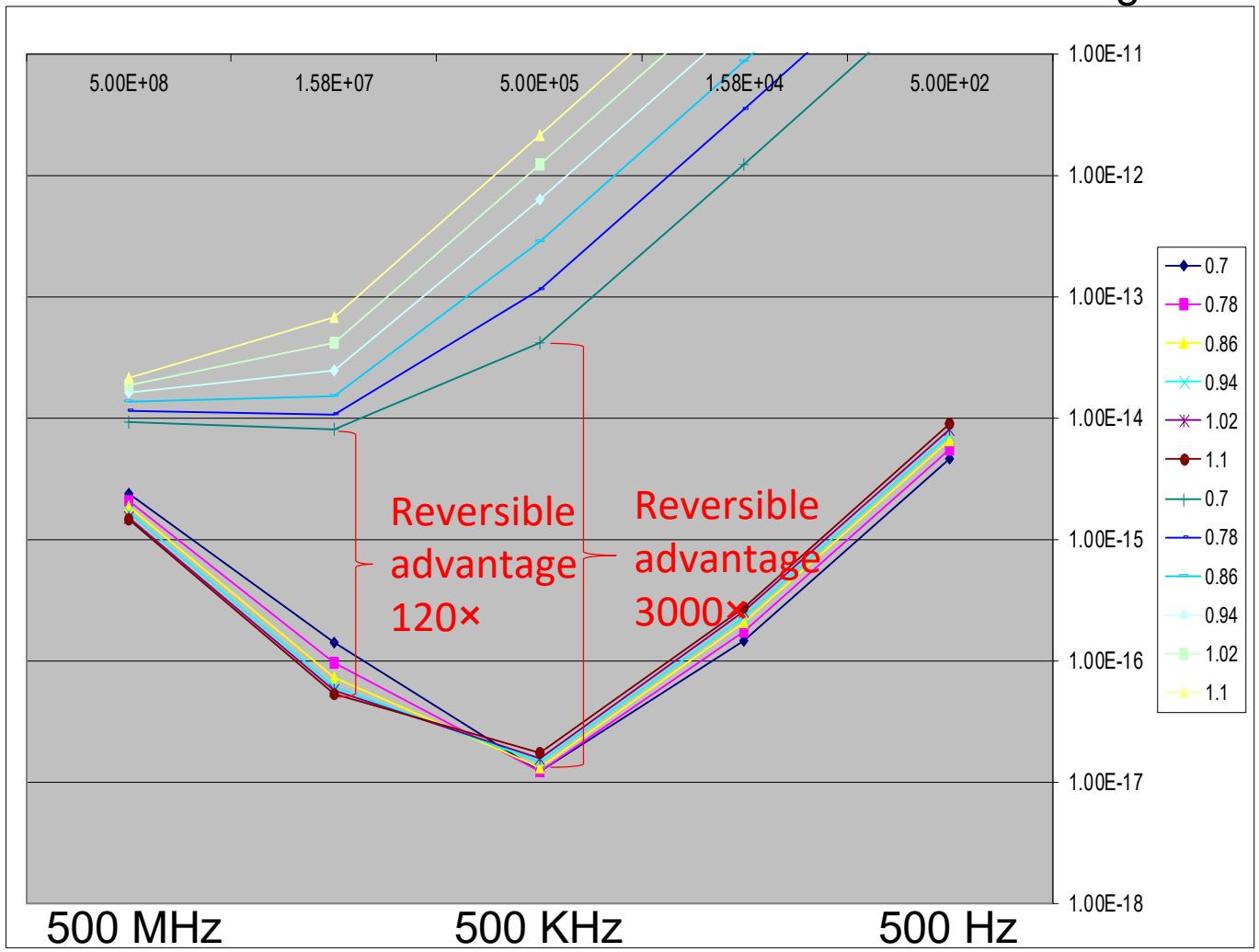
1440 nm width

Overlay animation



2880 nm width

Overlay animation



5760 nm width

Math I



- CMOS dissipation more complex than $\frac{1}{2}CV^2$
  - It's actually $\frac{1}{2}(C_g + C_w)^2$, where C_g is capacitance due to gates and C_w is capacitance due to wire
- Initially assume transistors are of minimal width
- Reversible dissipation is $2RC/\tau \times \frac{1}{2}CV^2$, but there is more to the "energy factor" $2RC/\tau$ than meets the eye
  - It's actually $2R_{on}(C_g + C_w)/\tau$, but $R_{on} \times C_g$ is nearly constant under transistor width scaling
  - So, widening a minimal-size transistor by 2× will decrease resistance nearly by 2× but will cause little change in $(C_g + C_w)$

Math II



- If we increase width from minimum size up
  - CMOS's $\frac{1}{2}CV^2$ increases slightly
  - A reversible circuit's $2RC/\tau$ decreases a lot
- Thus increasing transistor width
  - increases the advantage of reversible over CMOS and
  - decreases absolute reversible dissipation
- This behavior persists until $C_g \approx C_w$
- Example in subsequent slides

Conclusion



- CMOS designers associate large, high drive transistors with the high-speed, high-power portion of the operating envelope
- Reversible logic designers should be aware that large transistors reduce power consumption
- The ubiquitous energy dissipation chart delivers an incomplete message
  - Example in this deck shows a hidden variable can be responsible for a 10× error
  - However, lowest energy reversible circuit may involve large transistors and hence lower circuit density